

Project Name : A14IM01\_DDR3

Platform : Montevina Penryn(CPU)+Cantiga(NB)+ICH9M(SB)

PAGE	CONTENT
1.	INDEX
2.	SYSTEM BLOCK DIAGRAM
3.	POWER DIAGRAM & SEQUENCE
4.	GPIO & Power Consumption
5.	CPU Penryn 1/2
6.	CPU Penryn 2/2
7.	CLOCK GEN (ICS9LRS3165B)
8.	NB HOST/ VSS 1/5
9.	NB DDR BUS / GPU / PCIE 2/5
10.	NB DDR INTERFACE/ VSS 3/5
11.	NB I/O POWER 4/5
12.	NB GFX/ VCC/ NCTF POWER 5/5
13.	DDR3 SODIMM
14.	ICH9M RTC/ SATA/ HDA/ LPC 1/3
15.	ICH9M SYS/ GPIO/ PCIE/ USB 2/3
16.	ICH9M POWER 3/3
17.	EC IT8500BX / BIOS/KB CONN
18.	HDD/ ODD / MINI CARD
19.	CRT/LVDS/PWR SW
20.	LAN/CARD READER/15DB/JMC261
21.	TP/LED/WEBCAM/USB CHARGER
22.	CODEC/INT MIC/SPEAKER/92HD81
23.	EXT_MIC /HEADPHONE/USB/FAN
24.	DC IN/MDC/Discharge Resistor
25.	CPU CORE (OZ8291)
26.	0.75VS/+1.8VS/1.05V(OZ8116)
27.	+1.5VS/+5VA (OZ815)
28.	BATT IN/CHARGER(OZ8602)
29.	VCC SW/+3.3VA/HIGH-SPEED CAP
30.	Appendix Ver.A History

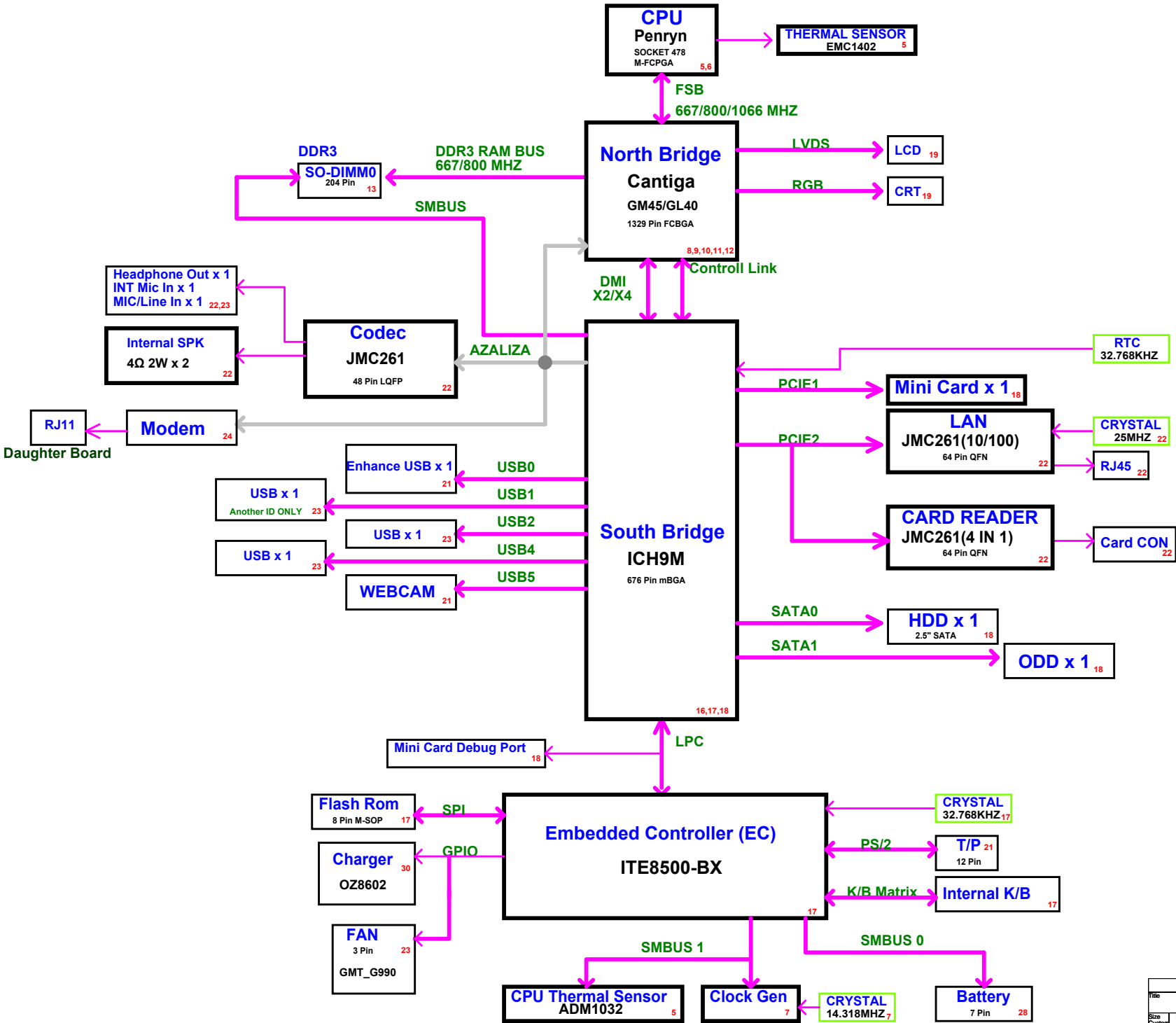
M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

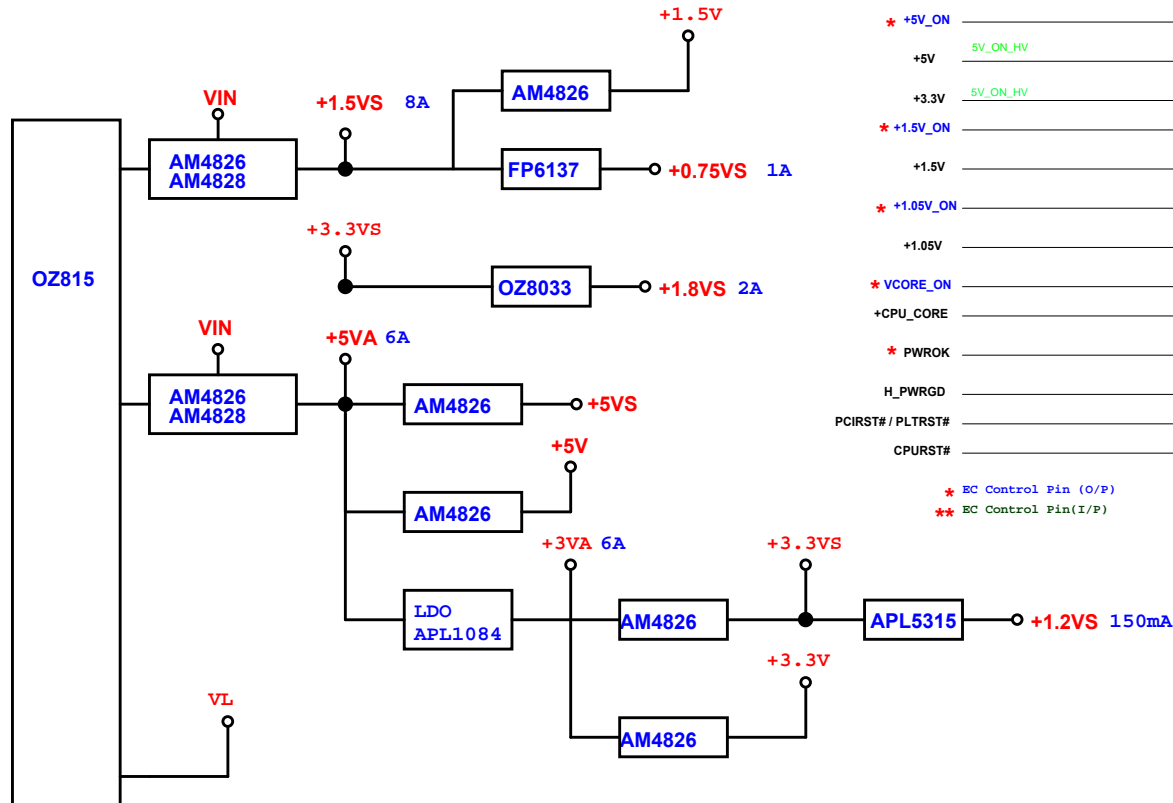
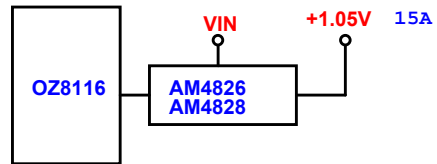
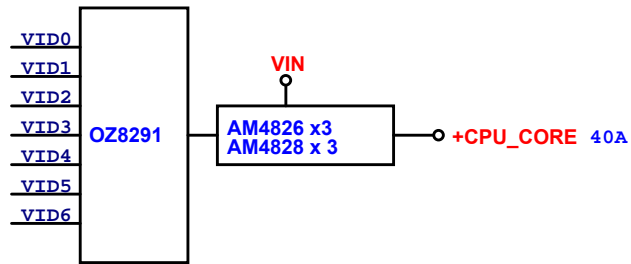
Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

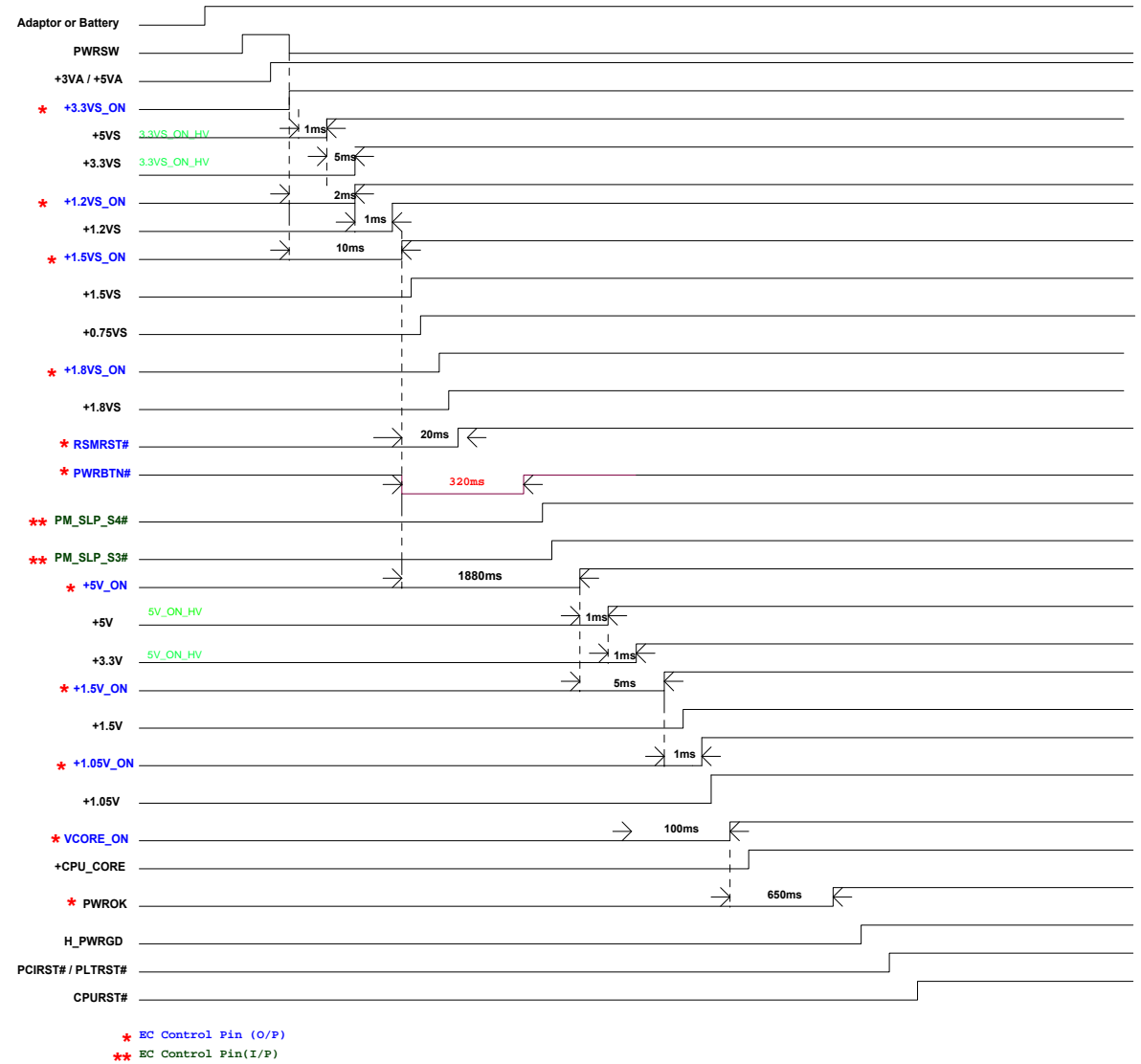
SYSTEM BLOCK DIAGRAM



# POWER BLOCK DIAGRAM



# System Poewr On Sequence



ICH9M GPIO	
GPIO0	PM_BM_BUSY#
GPIO1	EC_EXTSMI#
GPIO2	INT_PIRQE#
GPIO3	INT_PIRQF#
GPIO4	INT_PIRQG#
GPIO5	INT_PIRQH#
GPIO6	BIOS_REC
GPIO7	<b>N.C</b> (TACH3)
GPIO8	<b>N.C</b>
GPIO9	<b>N.C</b> (WOL_EN)
GPIO10	<b>N.C</b> (ALERT#)
GPIO11	SMB_ALERT#
GPIO12	LAN_PHYPC
GPIO13	<b>N.C</b> (GLAN_DOCK#)
GPIO14	<b>N.C</b> (NETDETECT)
GPIO15	PM_STPPCI#
GPIO17	<b>N.C</b> (TACH0)
GPIO18	<b>N.C</b>
GPIO19	SATA1GP
GPIO21	SATA0GP
GPIO22	<b>N.C</b> (SCLOCK)
GPIO23	LDRQ1#
GPIO24	CRB_SV_DET
GPIO25	PM_STPCPU#
GPIO26	PM_SLP_S4_STATE#
GPIO27	QRT_STATE0
GPIO28	QRT_STATE1
GPIO29	USB_OC#5
GPIO30	USB_OC#6
GPIO31	USB_OC#7
GPIO32	PM_CLKRUN#
GPIO33	HDA_DOCK_EN
GPIO34	<b>N.C</b> (HDA_DOCK_RST)
GPIO35	CLK_SATA_OE#
GPIO36	SATA2GP
GPIO37	SATA3GP
GPIO38	ODD_DET
GPIO39	ICH_GPIO39
GPIO40	USB_OC#1
GPIO41	USB_OC#2
GPIO42	USB_OC#3
GPIO43	USB_OC#4
GPIO48	MFG_MODE
GPIO49	H_PWRGD
GPIO50	PCI_REQ#1
GPIO51	PCI_GNT#1
GPIO52	PCI_REQ#2
GPIO53	PCI_GNT#2
GPIO54	PCI_REQ#3
GPIO55	PCI_GNT#3

ITE8510 GPIO		Default Pull/Mode
GPA0	RF_LED#	UP / GPI
GPA1	EC_BSEL1	UP / GPI
GPA2	BT_L_BEEP	UP / GPI
GPA3	WLAN_PWR#	UP / GPI
GPA4	P_ID0	UP / GPI
GPA5	P_ID1	UP / GPI
GPA6	PM_RSMRST#	UP / GPI
GPA7	EC_BL_PWM	UP / GPI
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	+1.05V_ON	Dn / GPI
GPB3	BAT_SMBCLK	/ GPI
GPB4	BAT_SMBDAT	/ GPI
GPB5	H_A20GATE	/ GPO
GPB6	H_RCIN#	UP / Funcl
GPB7	ENHANCE_USB#	Dn / GPI
GPC0	+1.5V_ON	Dn / GPI
GPC1	SMB_CLK_EC	/ GPI
GPC2	SMB_DAT_EC	/ GPI
GPC3	<b>N.C</b>	Dn / GPI
GPC4	SAVE_POWER	Dn / GPI
GPC5	SLP_S4_COY	Dn / GPI
GPC6	+3.3VS_ON	Dn / GPI
GPC7	CRT_DETECT	UP / GPI
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPI
GPD2	PLT_RST#	UP / Funcl
GPD3	<b>N.C</b>	UP / GPI
GPD4		UP / GPI
GPD5	PWR_USB_LED#	UP / GPI
GPD6	<b>N.C</b>	Dn / GPI
GPD7	SET_V	Dn / GPI
GPE0	LID#	Dn / GPI
GPE1	Fastcharge_EN	Dn / GPI
GPE2	PWROK	Dn / GPI
GPE3	Vcore_ON	Dn / GPI
GPE4	PWRSW	UP / GPI
GPE5	+1.2VS_ON	Dn / GPI
GPE6	WLAN_ON	Dn / GPI
GPE7	AMP_MUTE#	UP / GPI
GPF0	<b>N.C</b>	UP / GPI
GPF1	<b>N.C</b>	UP / GPI
GPF2	<b>N.C</b>	UP / GPI
GPF3	CHG_ON#	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	<b>N.C</b>	UP / GPI
GPF7	<b>N.C</b>	UP / GPI
GPG0	+3.3VA	Dn/GPO/TM
GPG1	+5V_ON	Dn/GPO/ID7
GPG2	<b>N.C</b>	
GPG6	WEBCAN_ON	Dn / GPI
GPH0	SAFETY_PROTECT	Dn/GPI/ID0
GPH1	+1.8VS_ON	Dn/GPI/ID1
GPH2	SENBAT_V	Dn/GPI/ID2
GPH3	CHG_G_LED	Dn/GPI/ID3
GPH4	CHG_R_LED	Dn/GPI/ID4
GPH5	BATOFF	Dn/GPI/ID5
GPH6	PWR_LED	Dn/GPI/ID6

ITE8510 GPIO		Default Pull/Mode
GPI0	<b>N.C</b>	/GPI/ADC
GPI1	LCDSW0	/GPI/ADC
GPI2	LCDSW1	/GPI/ADC
GPI3	<b>N.C</b>	/GPI/ADC
GPI4	BAT_I	/GPI/ADC
GPI5	BATT_TEMP	/GPI/ADC
GPI6	ADAPTOR_1	/GPI/ADC
GPI7	BAT_V	/GPI/ADC
GPJ0	EC_BL_ON	/GPI/DAC
GPJ1	EC_PROCHOT	/GPI/DAC
GPJ2	FAN_CTRL0	/GPI/DAC
GPJ3	CHG_REF	/GPI/DAC
GPJ4	CHG_I	/GPI/DAC
GPJ5	PM_THROTTLING#	/GPI/DAC

Penryn CPU				
	CPU CORE(V)	ICC(A)	W	TEMP(℃)
IMVP-6+	1.05	44.0	36	

Cantiga			
VCC	ICC(mA)	W	TEMP(℃)
+3.3V	262	0.87	105
+1.8VS	3249	5.73	
+1.5V	86	0.129	
+1.05	14688.52	15.43	

ICH9M			
VCC	ICC(mA)	mW	TEMP(℃)
+5V	4	20	70
+5VS	2	10	
+3.3V	347	1145.1	
+3.3VS	212	699.6	
+1.5V	1988	2982	
+1.05V	1634	1715.7	

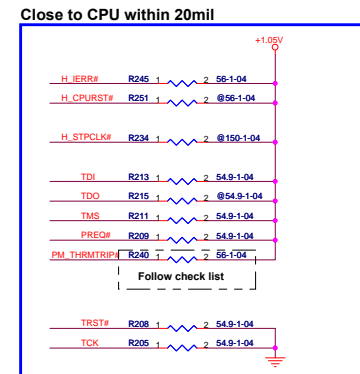
ITE8500			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3V	100	330	70

CLOCK GENERATOR			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3V	1000	3300	70

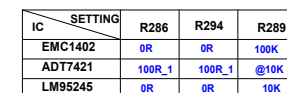
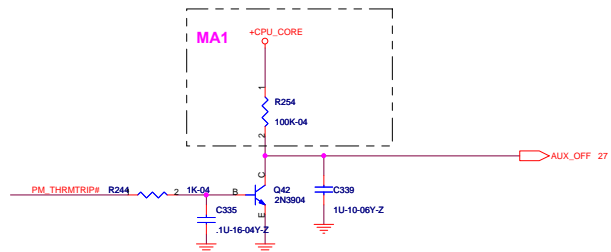
IDT92HD81			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3V(DVDD)	200	660	70
+5V(AVDD)	1000	5000	

ADM1032			
VCC	ICC	mW	TEMP(℃)
+3.3V	170uA	0.56	150

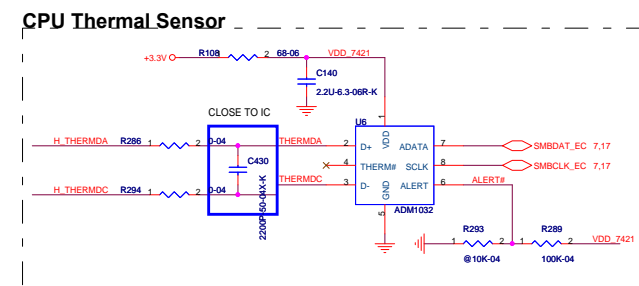
JMC261			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3VS	300	990	70
+1.2VS	150	180	

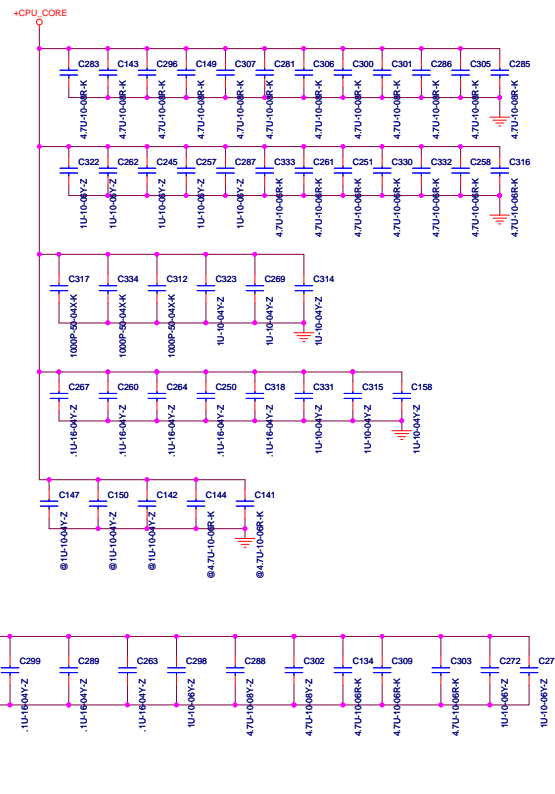


FSB \ BSEL	BSEL2	BSEL1	BSEL0	MHZ
FSB667	0	1	1	166
FSB800	0	1	0	200
FSB1066	0	0	0	266

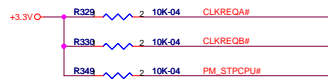


R289 can use 100K for 3 vender real application  
R286,R294 can use 0-04 for ADT7421 real application

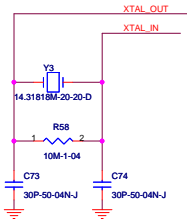
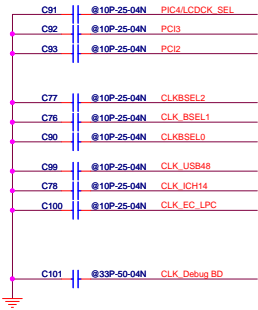




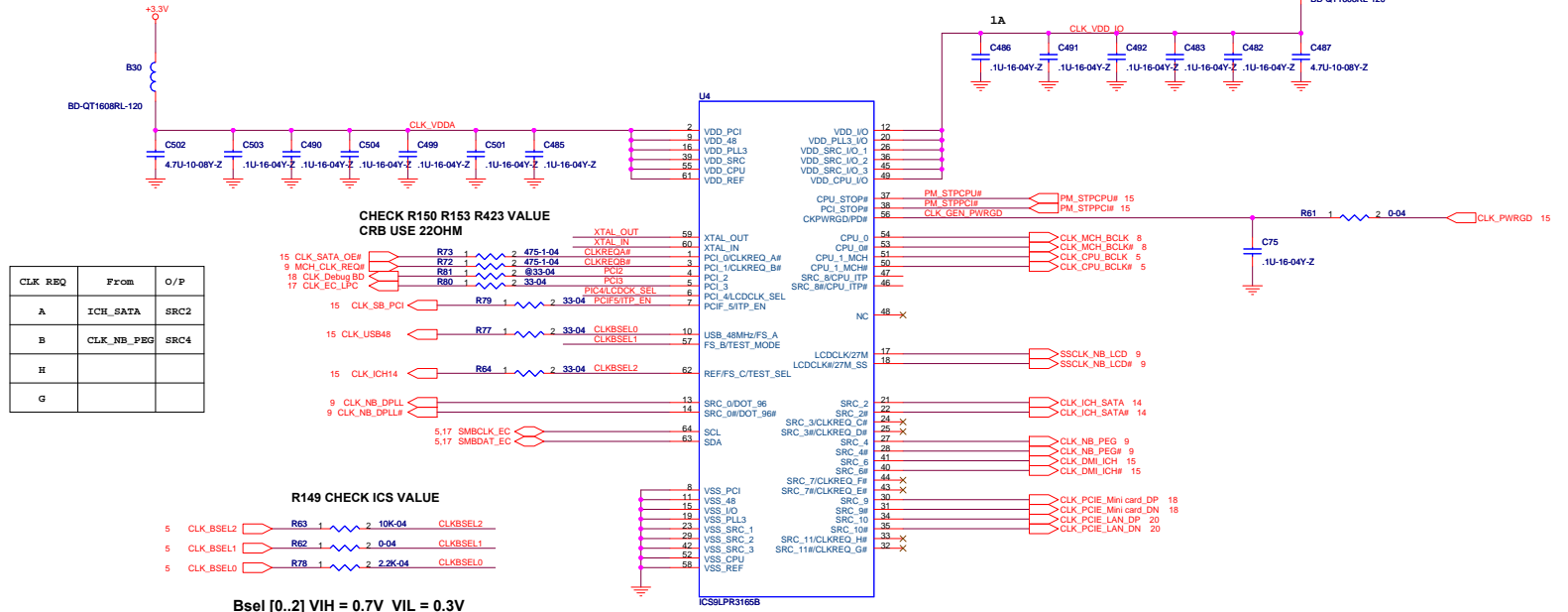
<b>SHUTTLE INC</b>			
Title			
<b>A14IM01</b>			
Size	Document Number	Rev	
Custom	<b>CPU Penryn 2/2</b>	<b>A</b>	
Date:	Tuesday, November 24, 2009	Sheet	6 of 30



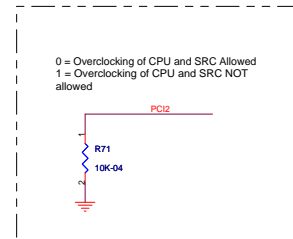
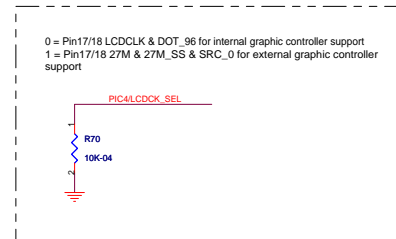
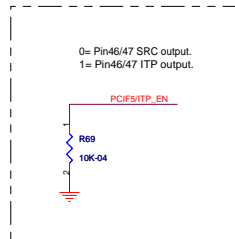
Reserved FOR EMI

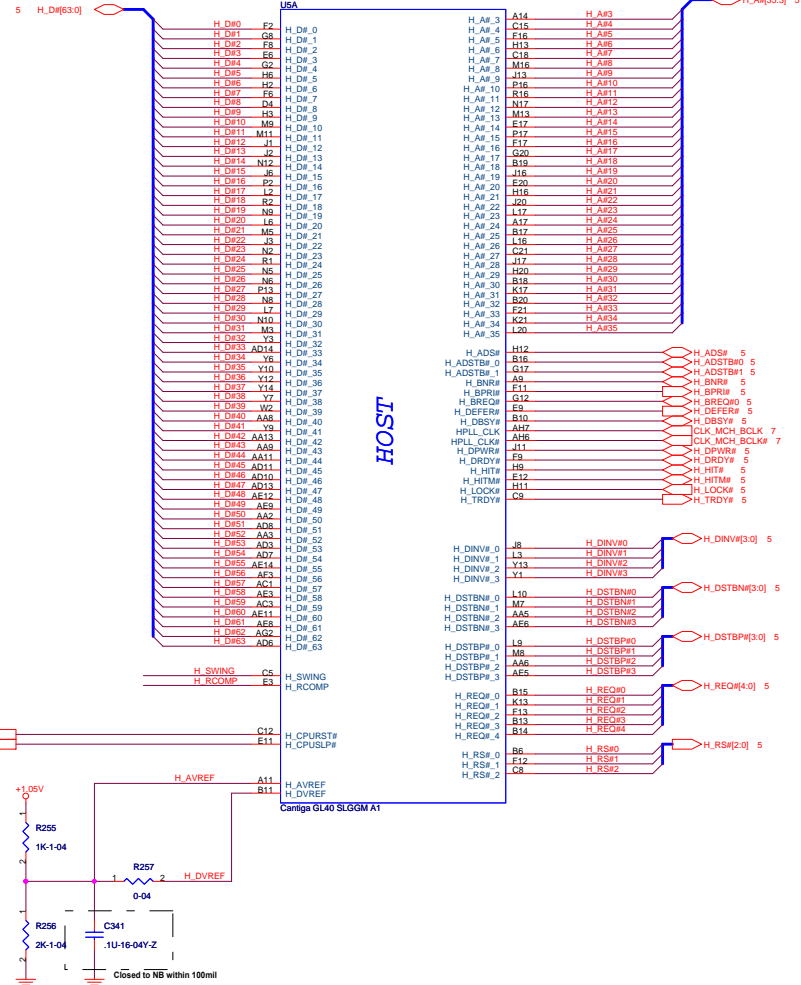
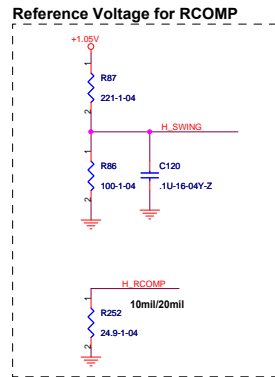
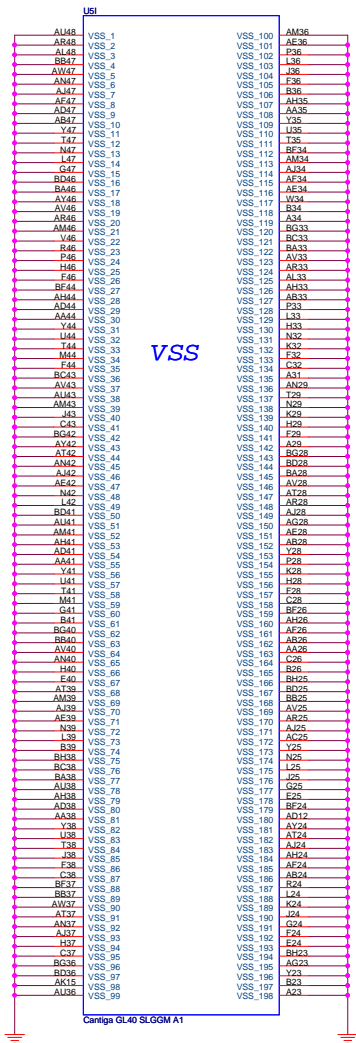


$C_e = 2 * C_L - (C_s + C_i)$   
 $C_L$  = Crystal Load Cap = 20P  
 $C_i$  = IC internal Cap = 5P  
 $C_s$  = 2P  
 $C_e$  = Crystal external Cap = 33P



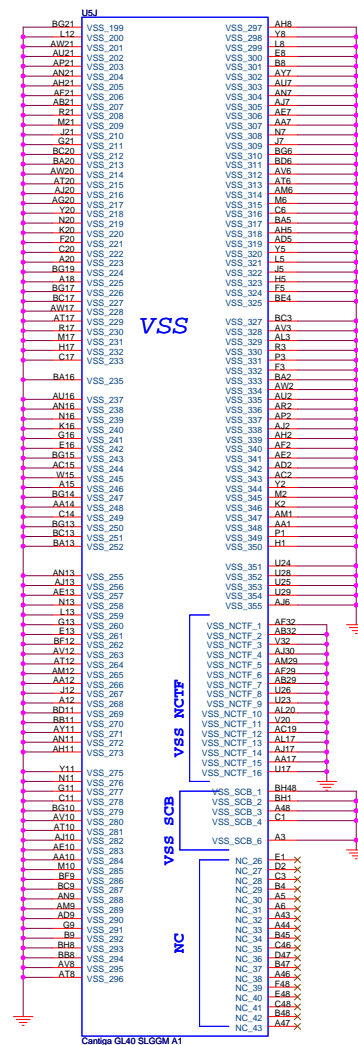
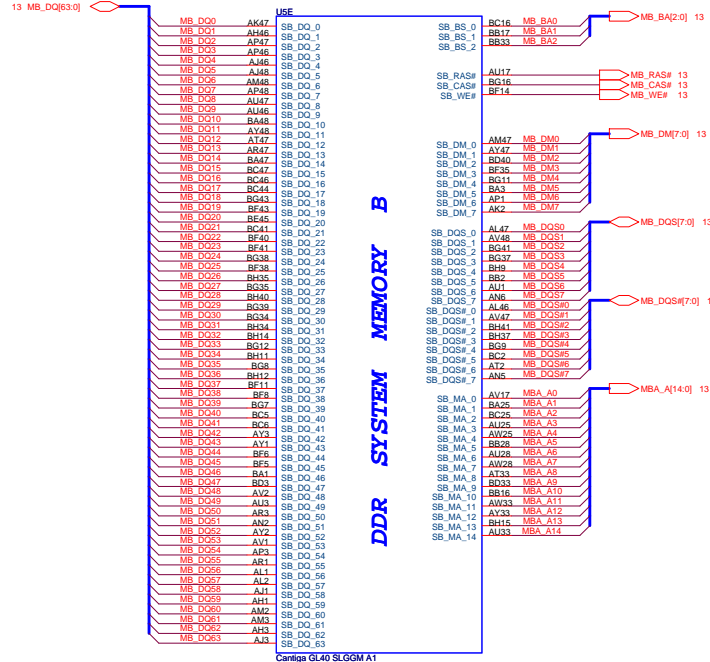
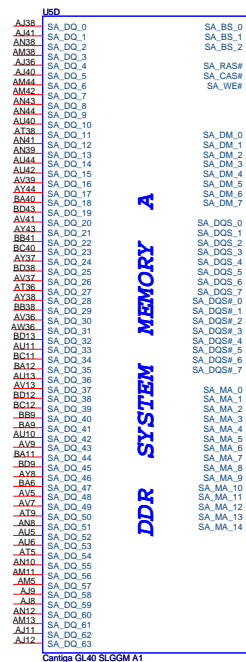
\*Need reserved space for 72Pin CLOCK GEN\*

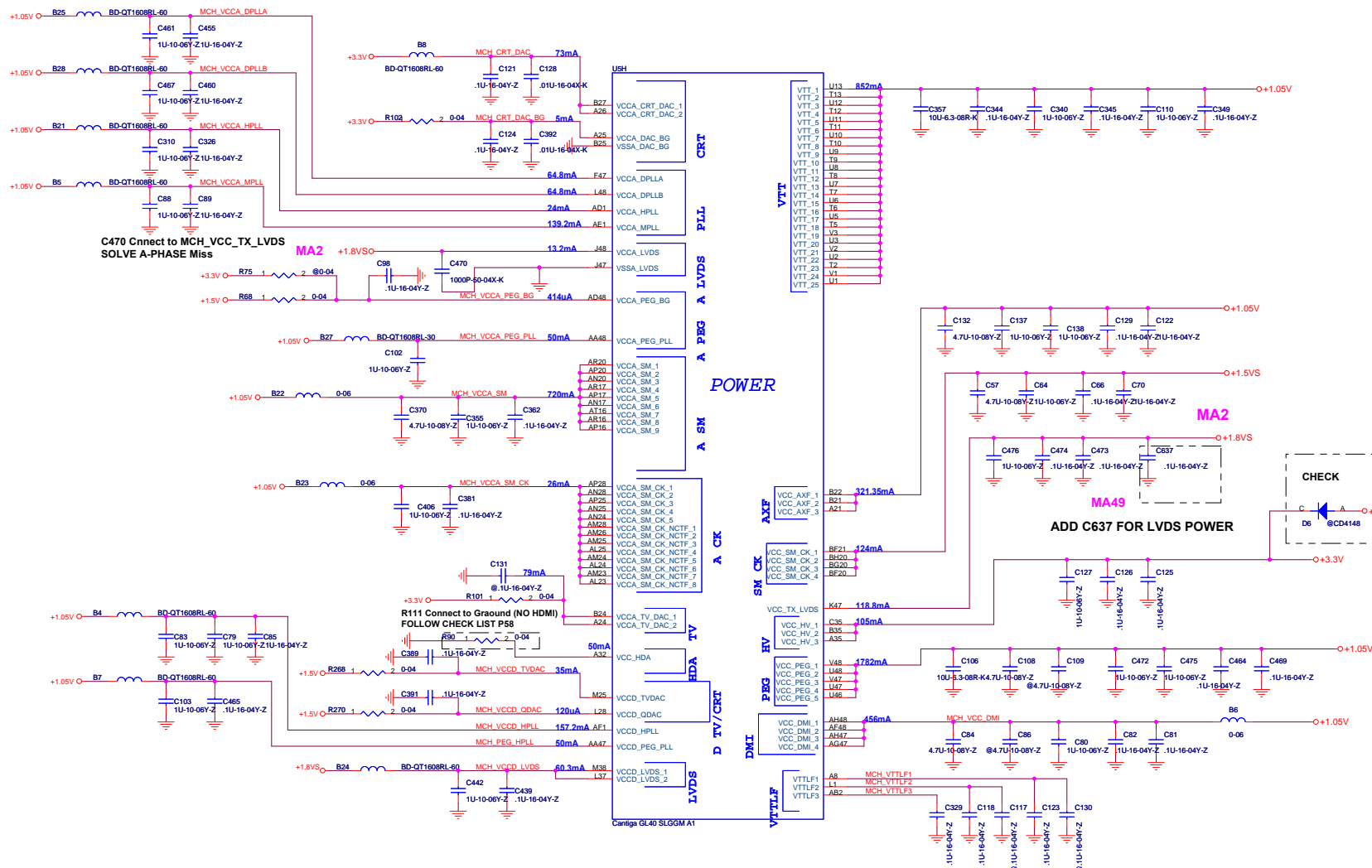








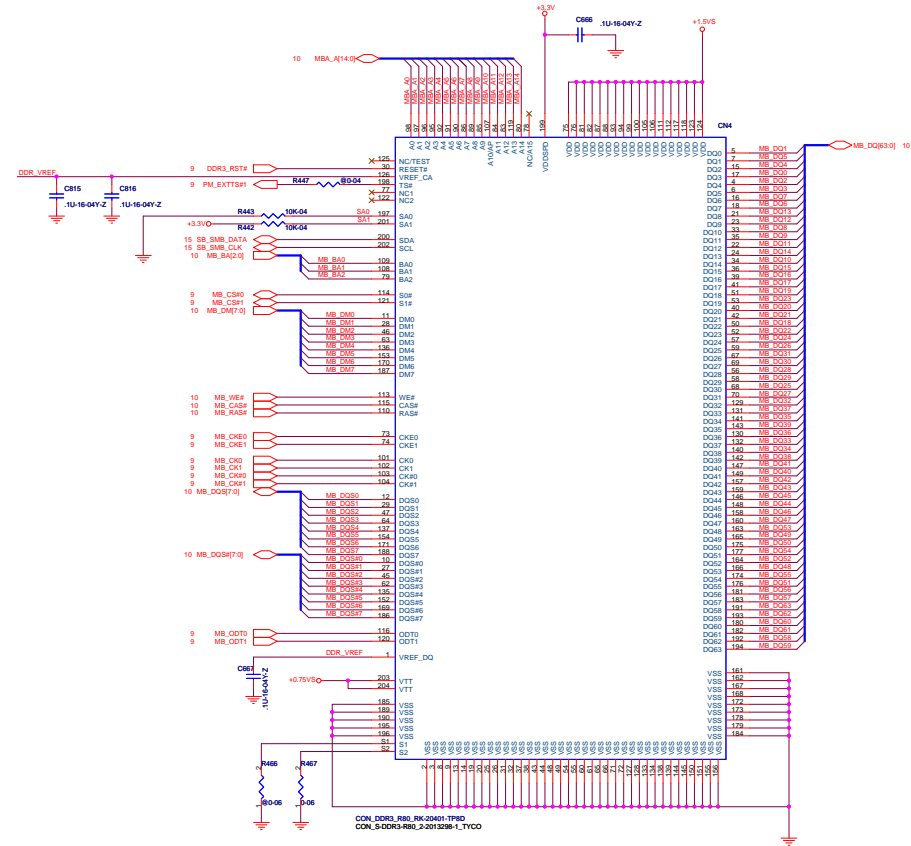
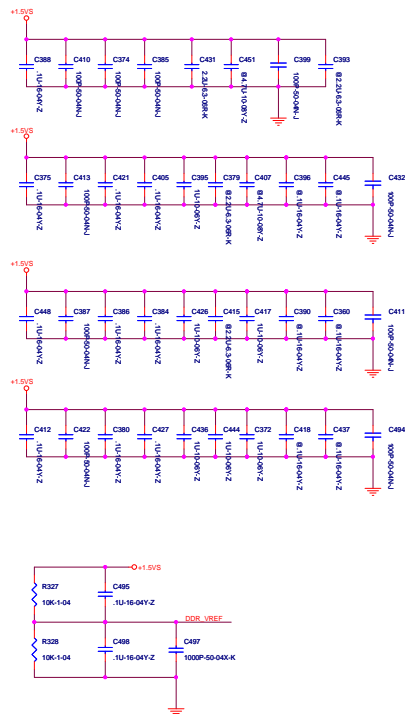


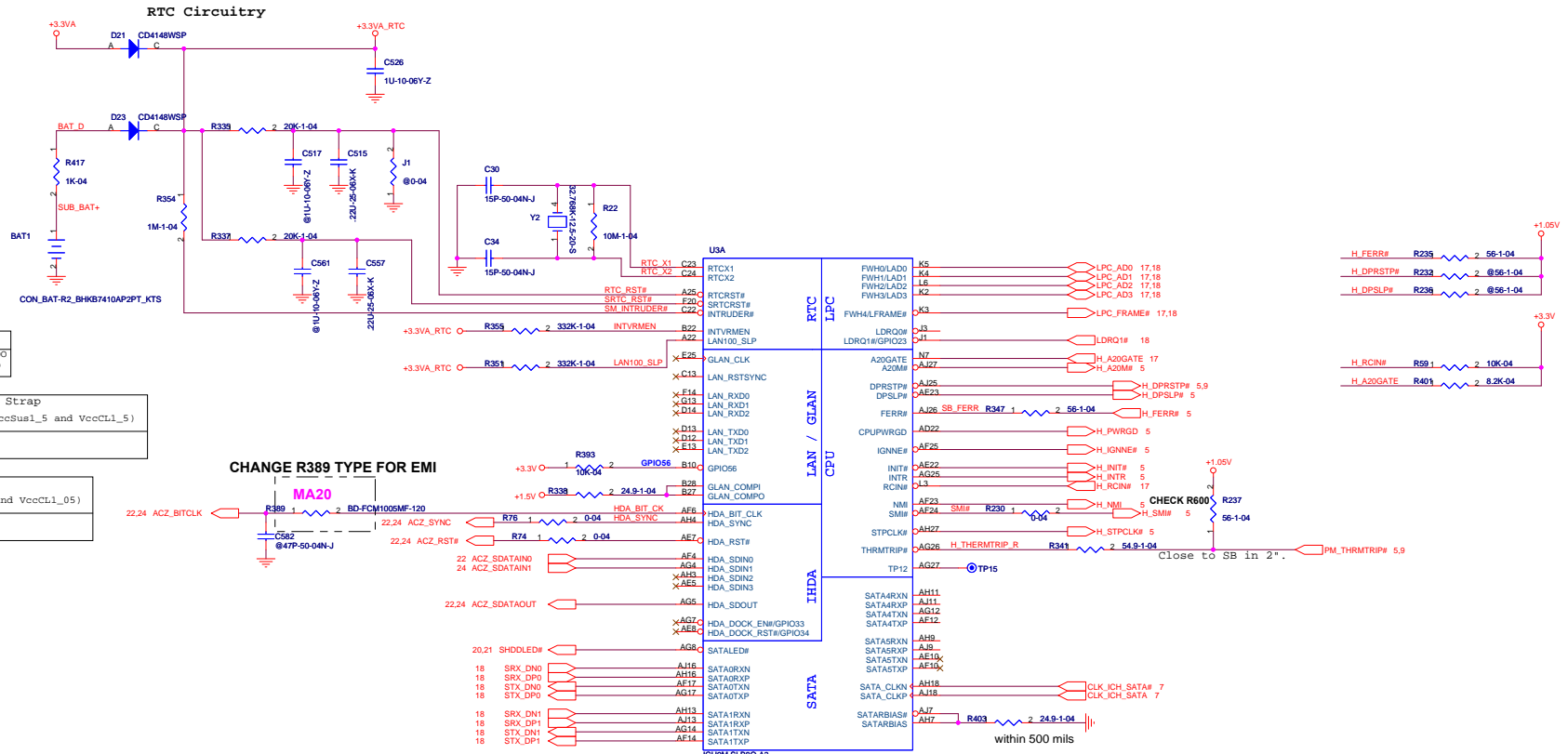




## DDR Termination

The diagram illustrates the termination of a 33-MHz signal path. It shows two 33-MHz buffers, MS\_C12SPR\_04 and MS\_C12SPR\_04, connected to a 33-MHz clock source. The buffers are terminated with 33-ohm resistors. The diagram also shows the connection of the buffers to the DDR memory array, which is terminated with 33-ohm resistors. The termination is implemented using a 33-ohm resistor network connected to the 33-MHz clock source.

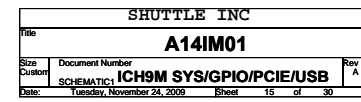




SM\_INTRUDER#  
0 = Disable Internal 1.5Vs LDO  
1 = Enable Internal 1.5Vs LDO

ICH9-M Internal VR Enable Strap  
(Internal VR for VccSusi\_05, VccSusi\_5 and VccCL1\_5)  
Low = Internal VR Disabled  
High = Internal VR Enabled  
(Default)

ICH9-M LAN100\_SLP Strap  
(Internal VR for VccLAN1\_05 and VccCL1\_05)  
Low = Internal VR Disabled  
High = Internal VR Enabled  
(Default)



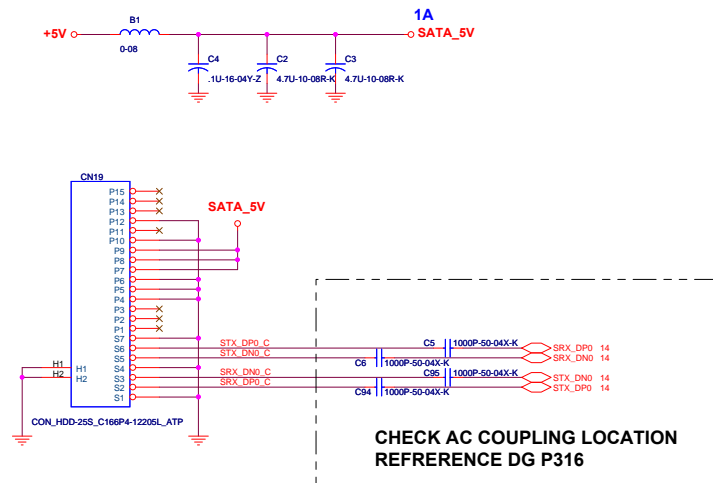




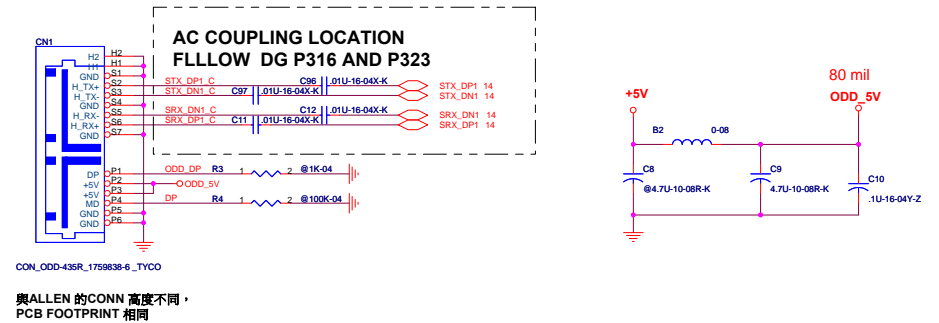




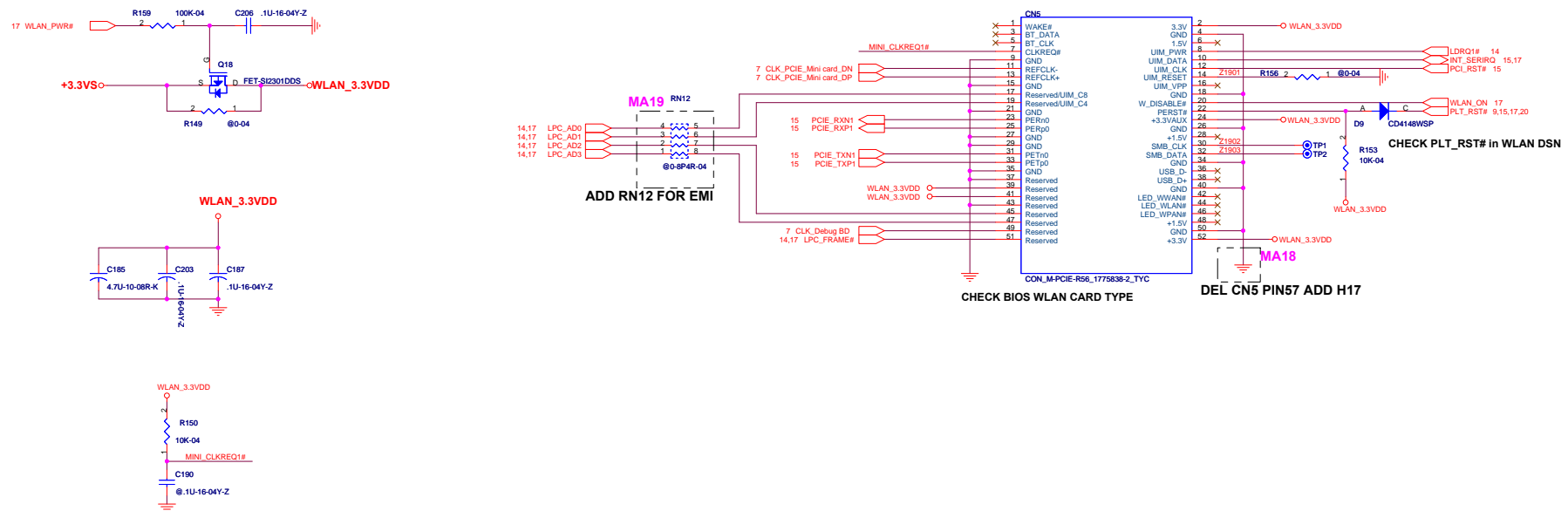
## SATA-HDD



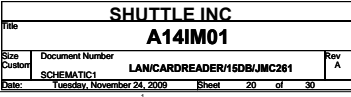
## CR-ROM



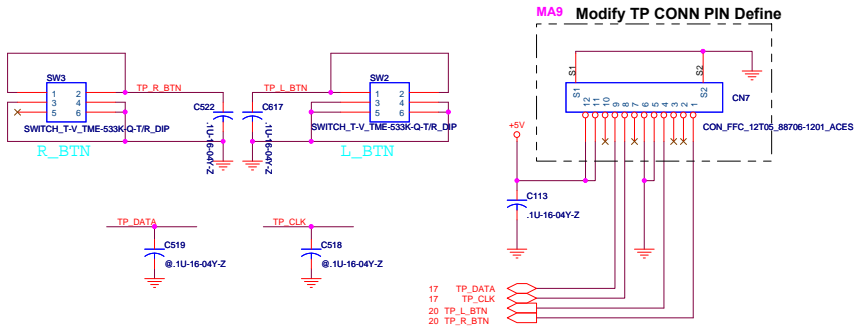
## MINI CARD CONN



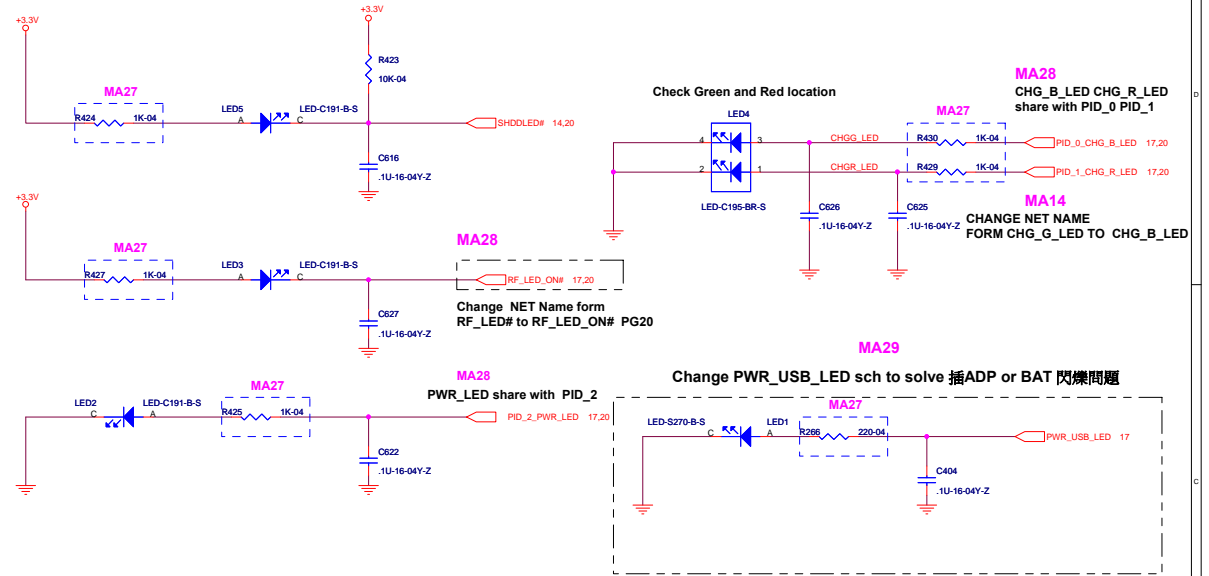




## Touch Pad

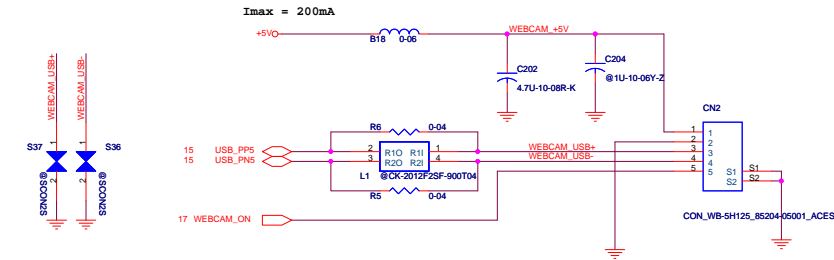


## LED MA27 - R424,R427,R425,R430,R429,R266 Change to 220-04

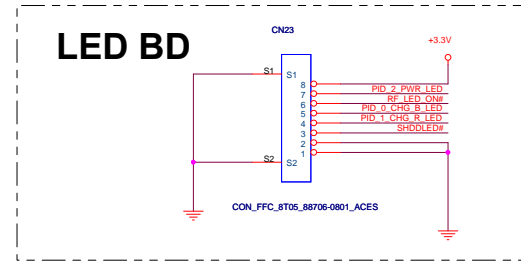


## WEBCAM CON

WEBCAM_ON	
1	ON
0	OFF

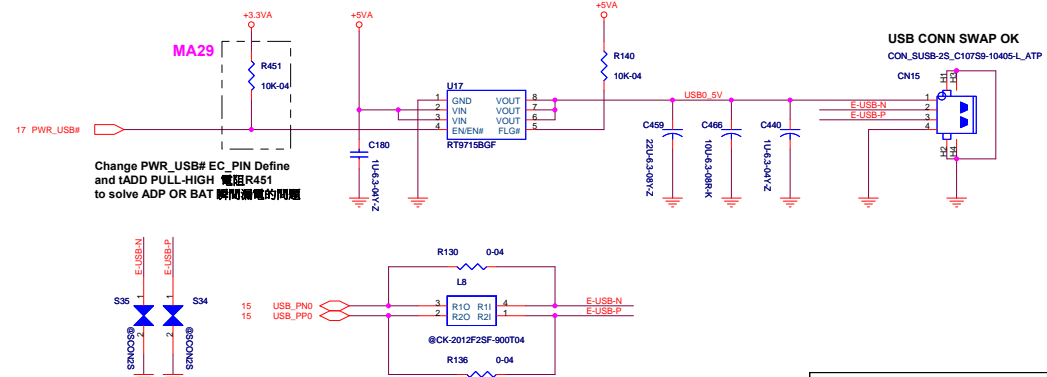


## LED BD



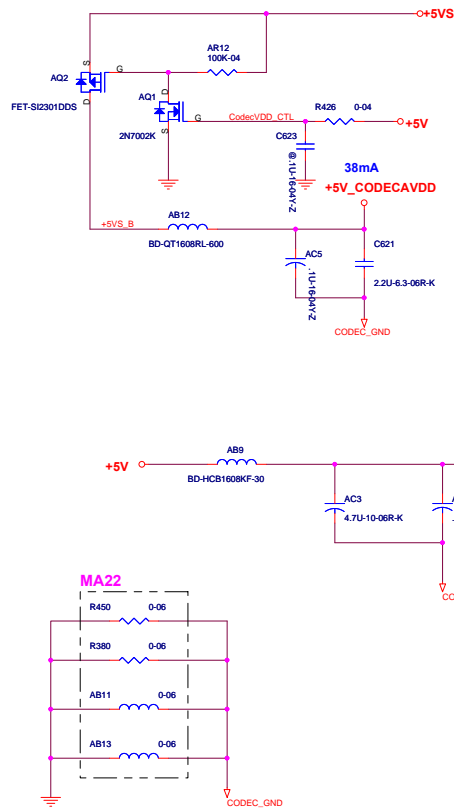
- MA14 ADD LED CONN CN23
- MA28 Change CN23 PIN7 NET Name form RF\_LED# to RF\_LED\_ON# PG20
- CHG\_B\_LED CHG\_R\_LED PWR\_LED share with PID\_0 PID\_1 PID\_2
- MA14 CHANGE CN23 PIN5 DEFINE FORM CHG\_G\_LED TO CHG\_B\_LED

## ENHANCE USB Port

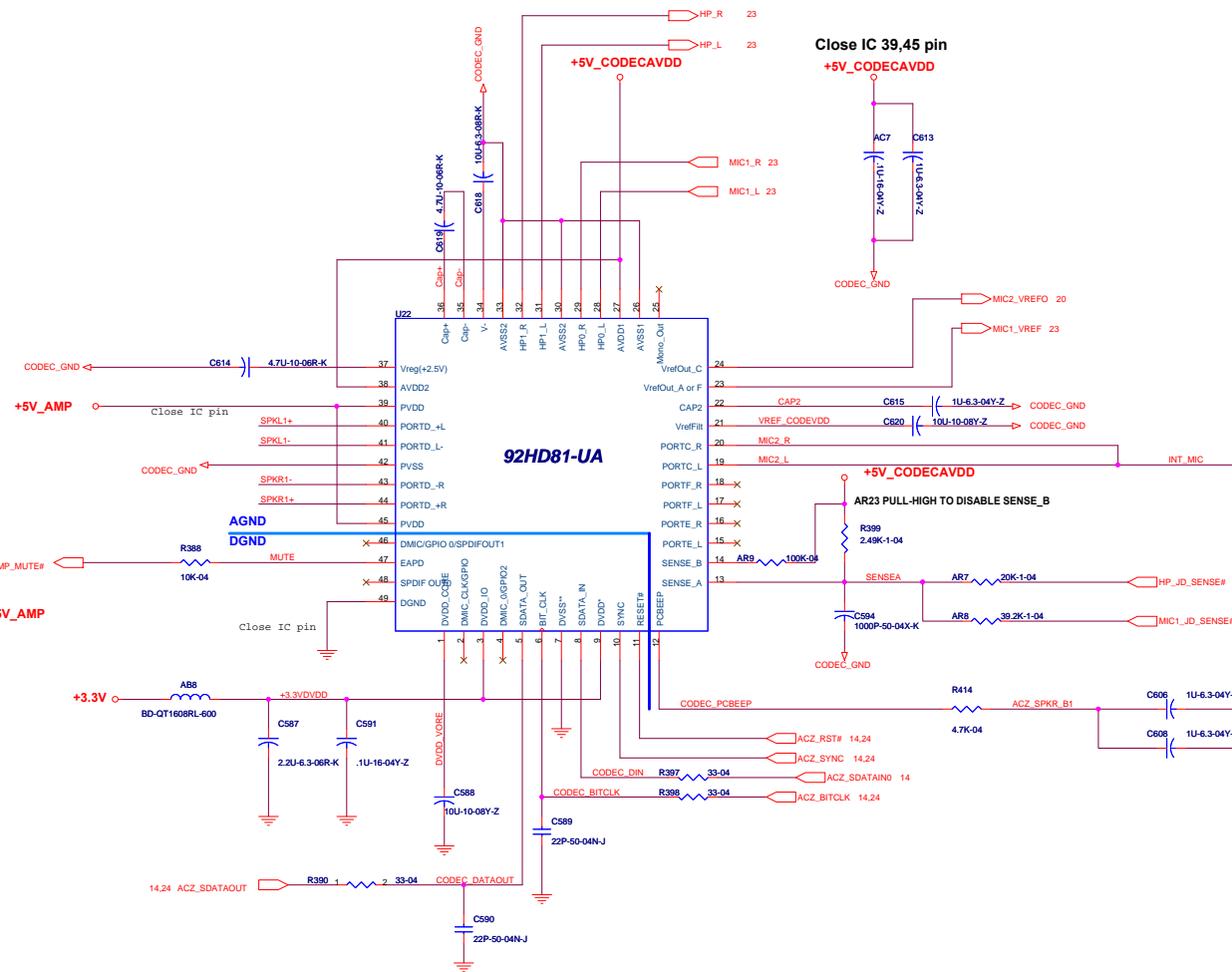


**CODEC 92HD81**

**AMP VDD**



**CHANGE R450,R380,AB11,AB13 to 0ohm for EMI**

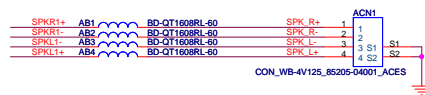
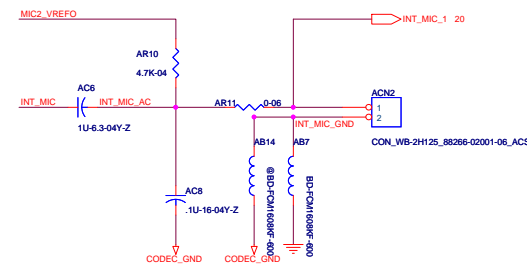


**SENSE\_A Channel**

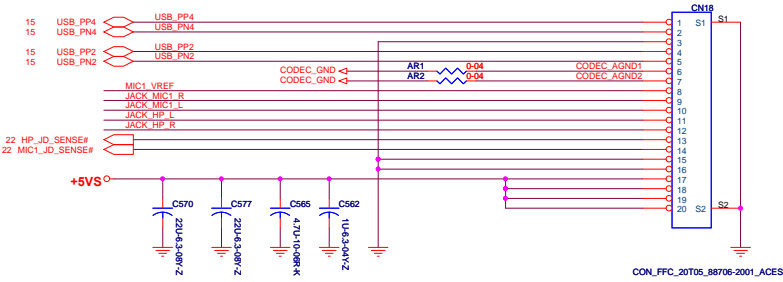
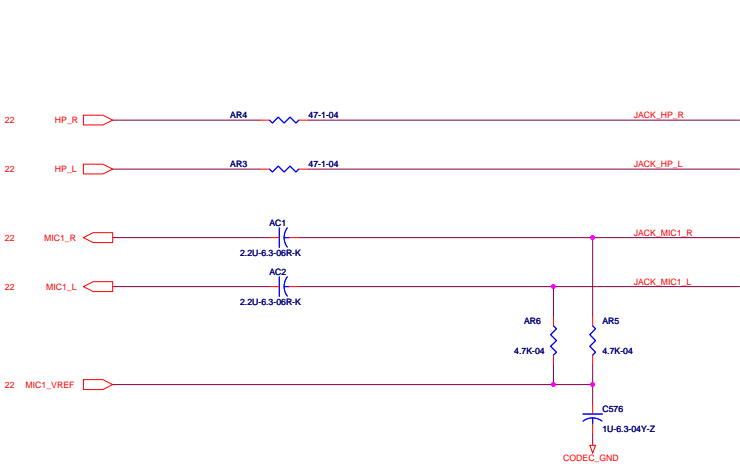
HP0-MIC-IN LINE-IN  
HP1-HEADPHONE-OUT LINE-OUT

39.2K PORTA HP0  
20K PORTB HP1

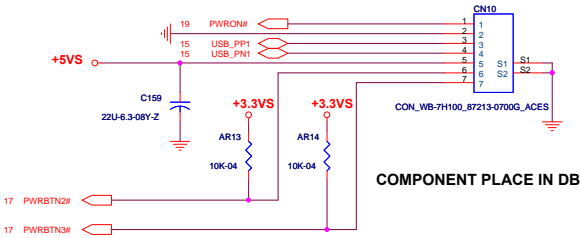
## INT\_SPEAKER

**INT\_MIC**

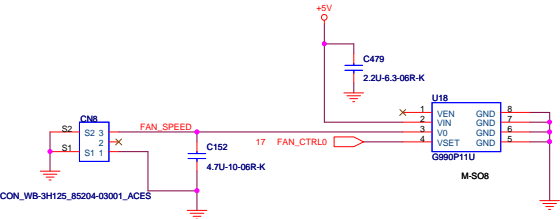
# EXT MIC/EXT Line In/ EXT USB JACK



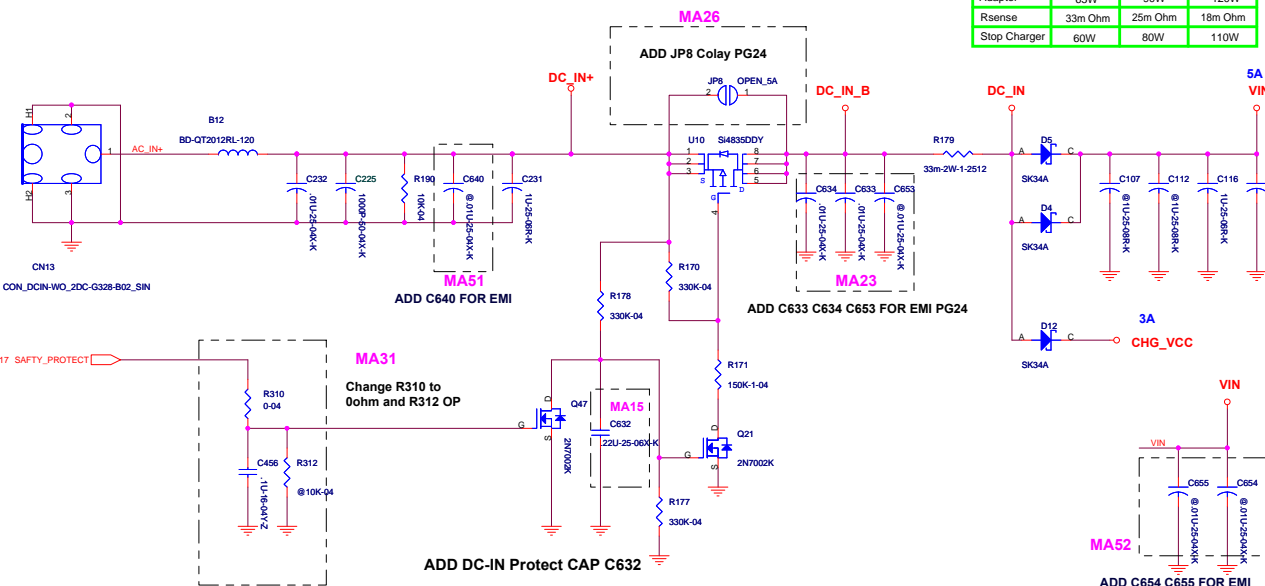
## EXT USB PORT 4



## CPU FAN CONTROL

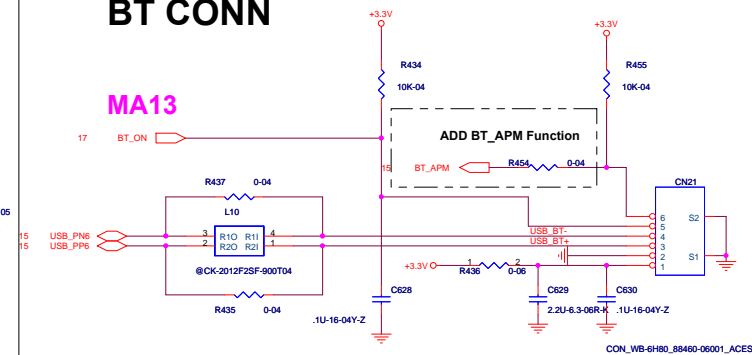


# DC IN



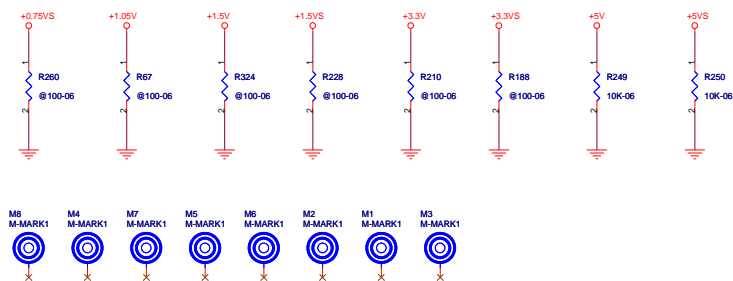
PROJECT	F50I0	F50I0	F50I5
Adaptor	65W	90W	120W
Rsense	33m Ohm	25m Ohm	18m Ohm
Stop Charger	60W	80W	110W

# BT CONN

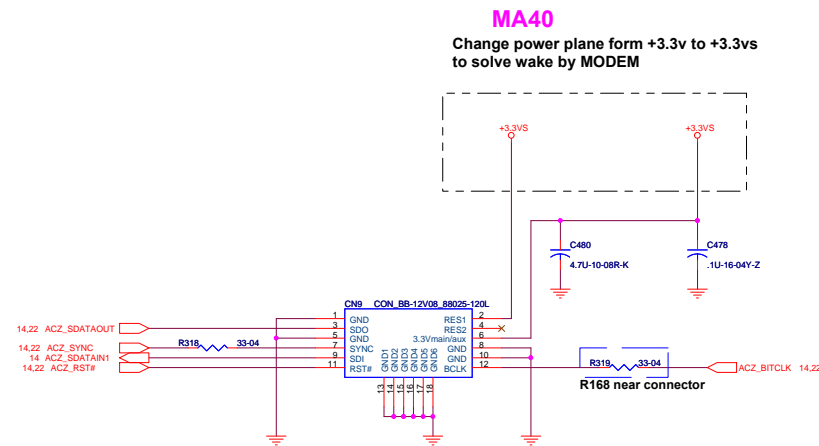


CHECK BT TYPE AND Life power function

# Discharge Resistor



# MDC





VID: 0.8~1.175V  
Icc max: 40A  
LLS: set to 2.1mV/A

ADD R432 Pull-High to +3.3V in DELAY\_VR\_PWRGOOD solve open issue

B16 上件 , JP2 OPEN FOR EMI

CHECK BATTERY Leacking current

MA45 ADD C641 C642 FOR EMI

OCP:50A

MA45 Change C201 to 0402 type

DEL-CSN-Connect-to-GND NET

MA45 ADD JP9 FOR EMI

Change C215 Location BY O2

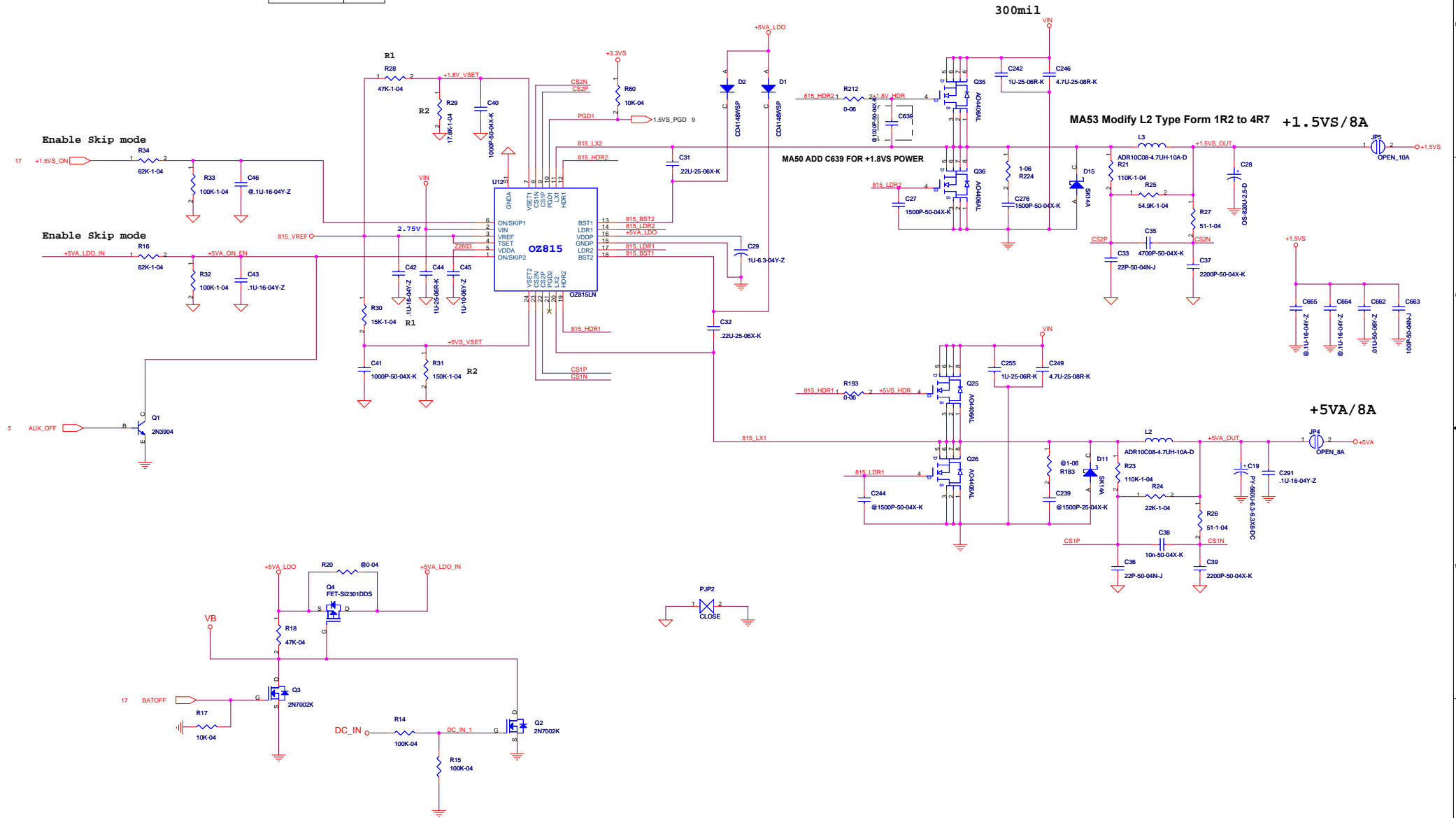
VID TABLE

	6	5	4	3	2	1	0	Vcore	Status
0	0	0	1	0	0	0	0	1.2875	(HFM)
0	0	0	1	1	0	0	0	1.2000	Boot Vout
0	0	0	1	1	1	0	0	1.1500	Merom(HFM)
0	1	1	0	1	0	1	1	0.8375	Y&M(LFM)
0	1	1	1	1	0	1	1	0.7625	Y&M(Deeper Sleep)
1	1	1	1	1	1	1	1	0.0000	Shut down



+1.8V/+5V_ON Voltage	Mode
<0.4V	OFF
>0.6V	PWM
>2.1V	SKIP

$$\text{Output Voltage} = \left[ \frac{V_{\text{ref}} \times R2}{R1 + R2} \right] \times 2$$



[illegible]

Vichg =RAD1\*Irsense\*10



The diagram shows two voltage divider circuits. The first circuit for **BAT+** uses resistors **R162** (931K-0.1-04) and **R169** (133K-0.1-04) with a capacitor **C420** (1U-10-04Y-2D45) to provide a **BAT\_V** signal (pin 17). The second circuit for **SENBAT+** uses resistors **R163** (100K-04) and **R311** (1K-1-04) with capacitors **Q46** (2N7002K) and **C450** (1U-10-08V-Z) to provide a **SENBAT\_V** signal (pin 17). Both circuits are powered by **BAT+** and ground.

**BAT+**  
 R162  
 931K-0.1-04  
 R169  
 133K-0.1-04  
 C420  
 1U-10-04Y-2D45  
 2N7002K  
 BAT\_V 17  
 BAT\_V\_ON#  
 Q46  
 2N7002K  
 R311  
 1K-1-04  
 SENBAT\_V 17  
 C450  
 1U-10-08V-Z  
 R309  
 220K-04

17.6V->BAT\_V=2.2V  
 16.8V->BAT\_V=2.1V  
 13.2V->BAT\_V=1.65V  
 12.6V->BAT\_V=1.575V  
 9.0V->BAT\_V=1.125V

Charge / Discharge Detect

17 CHG\_REF

R48 20K-1-04

R53 1.5K-1-04

R158 0-06

C52 1U-6.3-04Y-Z

C51 1U-6.3-04Y-Z

R54 1.5K-1-04

R49 16.5K-1-04

U11A GS358SF

VIN

C221 @1000P-50-04X-K

C222 .1U-25-06Y-Z

BAT\_I

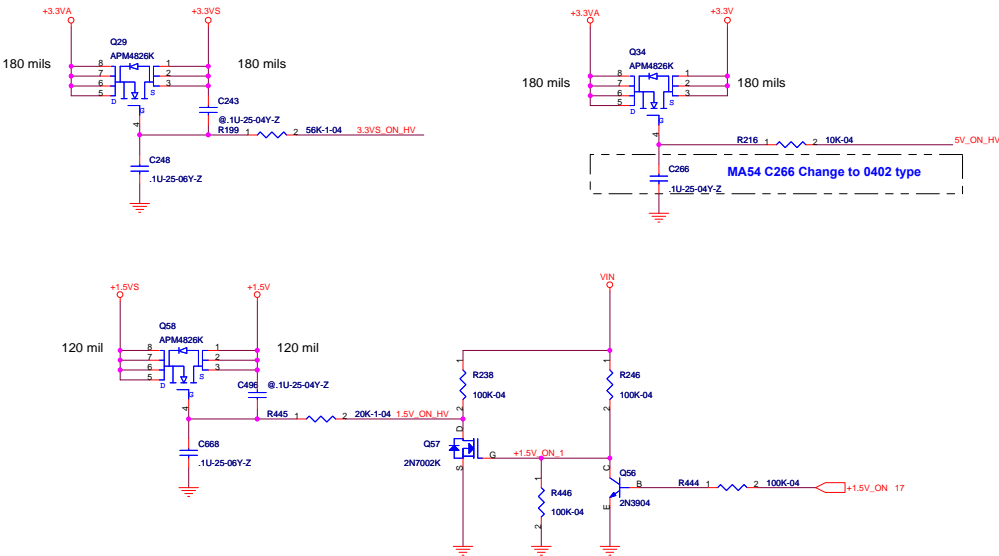
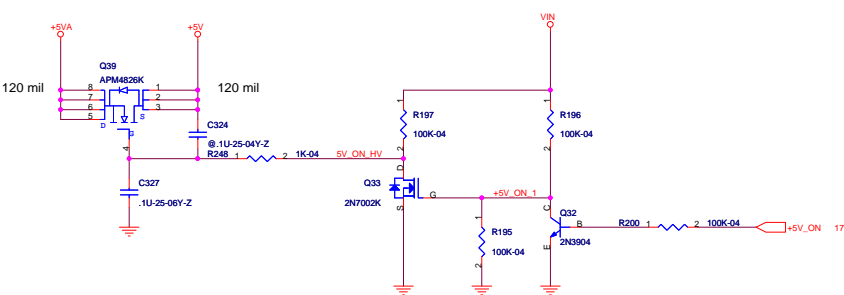
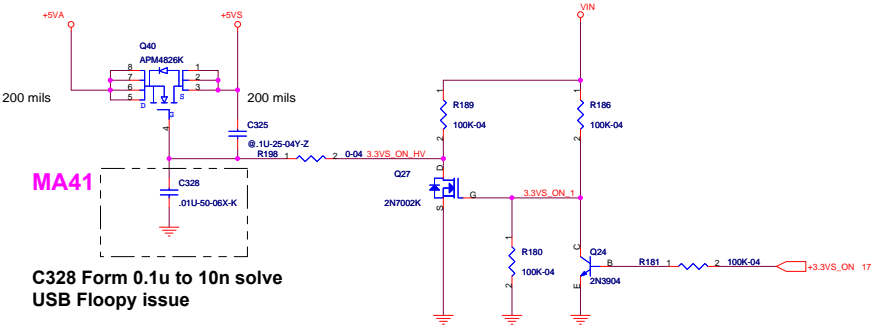
D10 M-SOD323

C224 @.1U-16-04Y-Z

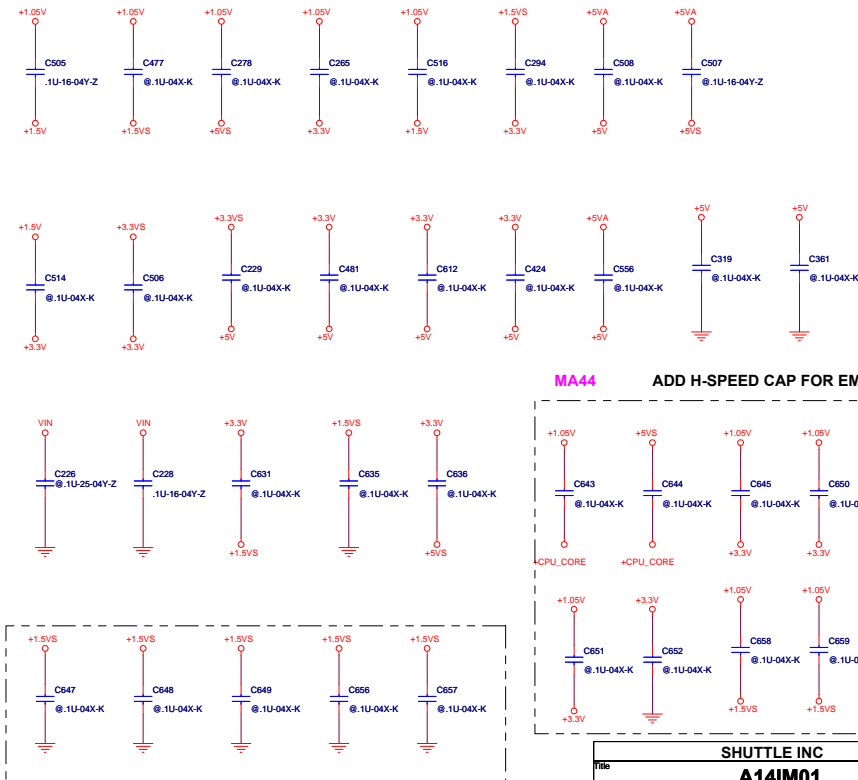
U10ZSNPTE-173.3B

CLOSE EC PIN

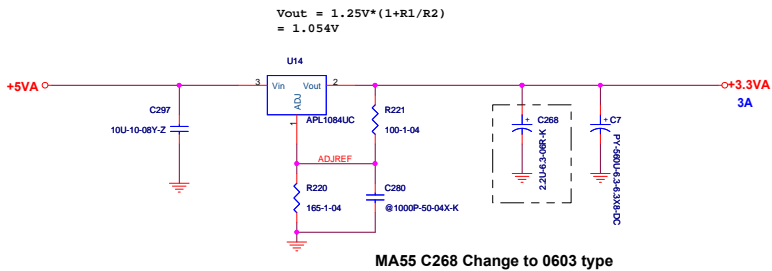
VCCSW



HIGH-SPEED CAP



LDO



RA to RB Modify list:

[illegible]